AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended) A single-poly EEPROM, comprising:

a first PMOS transistor serially connected to a second PMOS transistor, wherein the first and second PMOS transistors are both formed on an N-well of a P-type substrate, and wherein the first PMOS transistor includes a floating gate, a first P^+ doped drain region, and a first P^+ doped source region, the second PMOS transistor includes a gate and second P^+ doped source region, and the first P^+ doped source region of the first PMOS transistor serves as a drain of the second PMOS transistor; and

an N-type doped region formed in the P-type substrate beneath the floating gate serving as an erase gate ~~formed in the P-type substrate~~ in the vicinity of the first PMOS transistor, wherein the floating gate of the first PMOS transistor overlaps with the N-well and the P-type substrate and extends to the erase gate.

Claim 2 (canceled)

Claim 3 (currently amended) The single-poly EEPROM of claim [[2]]1 wherein the N-type doped region formed in the P-type substrate substantially does not overlap with the floating gate.

Claim 4 (currently amended) The single-poly EEPROM of claim [[2]]1 further comprising a floating gate oxide layer between the erase gate and the floating gate.

Claim 5 (currently amended) The single-poly EEPROM of claim 1 wherein when applying a pre-selected drain bias (V_d) to the second PMOS transistor, the floating gate of the first PMOS transistor obtains an induced voltage due to capacitance coupling effects, thereby turning on a P-channel under the ~~second~~ first PMOS transistor and obtaining a gate current near a maximum value.

Claim 6 (original) The single-poly EEPROM of claim 5 wherein V_d is about –5V.

Claim 7 (original) The single-poly EEPROM of claim 1 wherein the first PMOS transistor is a single-gate transistor without any control gate formed above the floating gate of the first PMOS transistor.

Claim 8 (currently amended) The single-poly EEPROM of claim 1 wherein when ~~operating~~ erasing the single-poly EEPROM, a pre-selected erase gate bias and a ~~first doped drain region voltage~~ bit line voltage (V_{BL}) are applied to the erase gate and the first P^+ doped drain region, respectively, so as to pull trapped electrons out of the floating gate by way of FN tunneling.

Claim 9 (currently amended) The operation of single-poly EEPROM as set forth in claim

8 wherein ~~phenomenon of over-erasing is avoided~~ at a beginning stage of an erasing operation, electrons trapped in the floating gate help to span the bit line voltage (V_{BL}) through entire channel region under the floating gate, thereby facilitating "pull-out" motion of the trapped electrons, as the erasing operation continues, ejection or erasing rate of the trapped electrons slows down due to disappearing channel caused by reduced electrons in the floating gate, thereby avoiding over-erase phenomenon of the single-poly EEPROM.

Claim 10(currently amended) The single-poly EEPROM of claim 8 wherein pre-selected erase gate bias is positive, and the ~~first doped drain region voltage~~ bit line voltage (V_{BL}) is negative.